REMARKS

In response to the action of August 9, 2006, applicant asks that all claims be allowed in view of the amendment to the claims and the following remarks.

Claims 1-30 are currently pending, claims 1, 6, 11, 16 and 21-26 being independent and claims 21, 22, 24, 26 and 29 having been withdrawn. In this amendment, claims 1-4, 6-9, 11-14, 16-19, 23 and 25 have been amended. Support for these amendments may be found in the application at, for example, page 7, line 25 to page 8, line 5 and Fig. 6. No new matter has been introduced.

Claim 23 has been rejected as being unpatentable over Chandrakasan (U.S. Patent No. 6,967,522). Applicant requests reconsideration and withdrawal of the rejection because Chandrakasan does not describe or suggest the subject matter of independent claim 23, as described more fully below.

As amended, claim 23 recites an electronic device that includes a first and second logic circuits, each having a thin film transistor over a substrate having an insulating surface. The electronic device also includes a detection means for detecting a first operating frequency of the first logic circuit that is electrically connected to the first logic circuit, and for detecting a second operating frequency of the second logic circuit that is electrically connected to the second logic circuit. The electronic device also includes a first threshold value control circuit electrically connected to the detection means; and a second threshold value control circuit electrically connected to the detection means. The first operating frequency is different from the second operating frequency.

Chandrakasan's disclosure is related to optimization of power utilization for integrated circuits. See Chandrakasan col. 1, lines 24-26. Chandrakasan discloses that electronic circuits can be designed to vary power consumption. See Chandrakasan col. 1, lines 42-43. In one example, Chandrakasan discloses that "microprocessors can be designed to vary their operational frequency as the processing demand on the device varies." See Chandrakasan col. 1, lines 43-45. Chandrakasan also discloses that "transistors may be fabricated on a silicon-on-insulator (SOI) wafer" and that "a buried gate structure can be used for threshold voltage control, rather than a direct access to a semiconductor substrate." See Chandrakasan col. 7, lines 26-31. Chandrakasan further discloses that "[i]n correspondence to present frequency data, the control

loop selects a supply voltage and a substrate voltage pair [and after converting the digital signal to an analog signal], apply the selected voltages to a device." See Chandrakasan col. 8, lines 56-62. In general, Chandrakasan uses an adaptive power supply and a substrate bias controller to control and reduce power consumption by selecting supply voltages and threshold voltages that are suited to operating conditions. See Chandrakasan col. 2, lines 45-50. More particularly, Chandrakasan discloses controlling power consumption by adjusting both a supply voltage and a threshold voltage in response to a present operating condition of the digital circuit. See Chandrakasan col. 2, lines 45-50.

As such, Chandrakasan does not describe or suggest many of the features recited by claim 23, as amended. For example, Chandrakasan does not describe or suggest first and second logic circuits, a second threshold value control circuit electrically connected to the detection means, a detection means for detecting a first operating frequency of the first logic circuit, and for detecting a second operating frequency of the second logic circuit, where the first operating frequency is different from the second operating frequency, as recited by claim 23.

This failure by Chandrakasan is not remedied by the mere assertions in the action that it would have been obvious to apply Chandrakasan's techniques to logic circuits, or use a detection means in Chandrakasan's system to detect an operating frequency. See action at page 2, lines 14-22. Mere assertions of this type are insufficient to establish a prima facie case of obviousness.

Accordingly, for at least these reasons, applicant respectfully requests reconsideration and withdrawal of the rejection of amended claim 23.

Claims 1-20, 25 and 28 have been rejected as being unpatentable over Chandrakasan in view of Skotnicki (U.S. Patent No. 6,555,482). Applicant requests reconsideration and withdrawal of the rejection because neither Chandrakasan, Skotnicki, nor any proper combination of the references describes or suggests the subject matter of independent claims 1, 6, 11, 16 and 25, as described more fully below.

Each of independent claims 1, 6, 11, 16 and 25, as amended, recites features similar to the features described above with respect to claim 23. For example, claims 1, 6 and 25 each recite an electronic device including first and second logic circuits, and a detection means which detects a first operating frequency of the first logic circuit and a second operating frequency of

the second logic circuit, where the first operating frequency is different from the second operating frequency. Claims 11 and 16 each recite an electronic device including first and second logic circuits, and a recording medium which detects a first operating frequency of the first logic circuit and a second operating frequency of the second logic circuit, where the first operating frequency is different from the second operating frequency.

For the reasons presented above with respect to claim 23, Chandrakasan, alone or in combination with the rejection's assertions of obviousness, does not describe or suggest the subject matter of amended claims 1, 6, 11, 16 and 25. In particular, Chandrakasan does not describe or suggest first and second logic circuits, and a detection means which detects a first operating frequency of the first logic circuit and a second operating frequency of the second logic circuit, where the first operating frequency is different from the second operating frequency, as recited by claims 1, 6 and 25. Nor does Chandrakasan describe or suggest first and second logic circuits, and a recording medium which detects a first operating frequency of the first logic circuit and a second operating frequency of the second logic circuit, where the first operating frequency is different from the second operating frequency, as recited by claims 11 and 16.

Skotnicki, which is cited in the action for disclosing a thin film transistor having a buried gate and a second gate, does not remedy the failure of Chandrakasan to describe or suggest the subject matter of claims 1, 6, 11, 16 and 25.

Accordingly, for at least these reasons, applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-20, 25 and 28.

Claims 27 and 30, which respectively depend from independent claim 1 and 23, have been rejected as being unpatentable over Chandrakasan in view of Skotnicki and Yamagishi (U.S. Patent No. 5,680,264). Yamagishi, which is said to disclose a frequency detection circuit having a counter and a discrimination circuit, does not remedy the failure of Chandrakasan or Skotnicki, alone or in combination, to describe or suggest the subject matter of independent claims 1 and 23.

Accordingly, applicant respectfully requests reconsideration and withdrawal of the rejection of claims 27 and 30.

Applicant submits that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Pursuant to 37 CFR §1.136, applicant hereby petitions that the period for response to the action dated August 9, 2006, be extended for one month to and including December 9, 2006.

The fee in the amount of $120.00 in payment for the Petition for the extension of time fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: December 7, 2006

Barbara A. Benoit
Reg. No. 54,777

Customer No.: 26171
Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331